

### **AMENDMENTS TO THE SPECIFICATION**

Please amend the following paragraphs:

**[0043]** Referring now to the drawings, where like elements are designated by like reference numerals, FIGS. 3-18 illustrate exemplary embodiments of methods of forming asymmetric transistor 100, 200, 300, 400, 500 (FIGS. 8, 11, 16, 17, 18) having a low threshold voltage  $V_t$  of about 0.3 V to about 0.7 V, more preferably of about 0.4 V to about 0.65 V, and as part of a three-transistor (3T) pixel sensor cell 101 (FIG. [[18]] 19). Although the embodiment of this invention will be described below with reference to a 3T CMOS imager, this is not to be taken as limiting. Accordingly, the invention also contemplates 4T, 5T, 6T, 7T CMOS imagers and CCD imagers. CCD imagers also contain reset and source followers transistors to which the present invention applies.

**[0048]** As shown in FIG. [[13]] 12, the source follower gate stack 136 comprises a first gate oxide layer 131 of grown or deposited silicon oxide, or of deposited high  $k$  insulator, on the silicon substrate 110, a conductive layer 132 of doped polysilicon or other suitable conductor material, and a second insulating layer 133, which may be formed of, for example, silicon oxide (silicon dioxide), nitride (silicon nitride), oxynitride (silicon oxynitride), ON (oxide-nitride), NO (nitride-oxide), or ONO (oxide-nitride-oxide). The first and second insulating layers 131, 133 and the conductive layer 132 may be formed by conventional deposition methods, for example, chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), among many others. While the second insulating layer 133 is advantageous, it is not required to enable this invention.